PATENT

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March 24, 2008
Date

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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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| Appl. No. | : 10/773,583 | Confirmation No. | : 6732 |
| Applicants | : Douglas A. Larson and Jeffrey J. Cronin | | |
| Filed | : February 5, 2004 | Attorney Docket No. | : 501296.01 (30266/US) |
| Art Unit | : 2188 | Customer No. | : 27,076 |
| Examiner | : Duc T. Doan | | |
| Title | : APPARATUS AND METHOD FOR DATA BYPASS FOR A BI-DIRECTIONAL DATA BUS IN A HUB-BASED MEMORY SUB-SYSTEM | | |

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**REPLY BRIEF UNDER 37 C.F.R. § 41.41**

Sir:

The applicants appealed the final rejection of claims 40-43 to the Board of Patent Appeals and Interferences on June 5, 2007, and an amended brief was filed on October 25, 2007. On January 22, 2008, the Examiner's Answer was issued. The applicants hereby submit this Reply Brief in accordance with 37 C.F.R. § 41.41 in response to the Examiner's Answer.

The Examiner contends that a read latency means the period of several clock cycles beginning when the memory device received the read command (the first clock cycle) and ends at the time when the memory device provides the beginning of the read data. The Applicants respectfully disagree. Rather, the Applicants contend that the read latency in a memory system comprising a bi-directional data bus begins when the memory controller issues a read command and ends when the memory controller receives the read data. The Zumkehr reference appears to agree with this definition by stating "the RAMBUS memory controller 210 defers write data transfer on a write command until the read latency of a previous read command is met. In this example, the write data 525A is not sent until time T6A which is when the read latency with respect to the read command 501A has been met." Column 6, lines 24-29. Thus, the Zumkehr reference is stating that the read latency for read command 501A begins at the time when the memory controller issues the read command 501A at time T1A and ends at the time that the read data is received by the memory controller at time T6A.

Although claim 40 does explicitly state providing write data to the bidirectional memory bus before the completion of the read latency of a previously issued read command, claim 40 does include the limitation. In particular, claim 40 requires issuing a read command, before completion of the read command, scheduling a write command, and prior to receiving the read data, providing write data corresponding to the write command to the bidirectional memory bus of the memory system. Therefore, and in other words, claim 40 requires providing write data to the bidirectional memory bus before the completion of the read latency.

Regarding Applicants' last line in section D of the Appeal Brief, Applicants intended the line to state "Therefore, the Zumkehr reference does not disclose or fairly suggest data bypass capabilities when a read command is issued, and before the read latency is met, issuing a write command and corresponding write [data]."

Finally, the Examiner contends that the previously issued write command 522B could have been issued at time T1A after issuing the read command 501B, and its corresponding data could have been issued at time T2A to time T3A. However, the Applicants contend that this would have resulted in a data collision on the SDRAM bi-directional data bus. See, Figure 2. The Zumkehr reference teaches that in response to the translator hub receiving a new write

command, a previously issued write command and corresponding write data will be sent from the translator hub to the memory device on the SDRAM buses. See, Zumkehr, abstract, col. 5, lines 36-44, and col. 7, lines 8-15. Therefore, if the previously issued write command 522B was issued at time T1A as the Examiner suggested, an even earlier stored write command and corresponding write data in the translator hub would be sent from the translator hub to the memory devices on the SDRAM bus just after time T2A to time T3A (just after the time the translator hub received write command 522B). However, at time T3A, read data 510B is put onto the SDRAM data bus going from the memory device to the translator hub. Therefore, this would result in a data collision as the earlier stored write data is going upstream on the SDRAM bus and read data 510B is going downstream on the SDRAM bus. See, Figure 2 and Figure 5B.

In addition, the Zumkehr reference teaches that the purposes of the write buffers in the translator hub is so that a write command can be sent from the memory controller to the translator hub without sending the corresponding write data with it. See, Zumkehr, abstract, col. 3, lines 1-8, col. 4, lines 45-67 to col. 5, lines 1-13, col. 5, lines 39-44. As mentioned above, the Examiner contends that the previously issued write command 522B could have been issued at time T1A after issuing the previous read command, and its corresponding write data could have been issued at time T2A to time T3A. However, since the Zumkehr reference states that the purpose of the write buffers are so that the write commands can be sent from the memory controller to the translator hub without sending the corresponding write data right after, this would result in a data collision on the RAMBUS data bus. See Figure 2. If the write data is delayed and not sent at time T2A to time T3A, then there would be a data collision on the RAMBUS data bus between the delayed write data and read data 515B. For instance, the write data would need to be in the translator hub before time marker T6A. If the write data is sent any time between time T3A and received by time T6A, the write data would collide with the read data 515B on the RAMBUS data bus (i.e., the write data would be going upstream to the translator hub and read data would be going downstream to the memory controller). See, Figure 2 and Figure 5B.

Therefore, based on the teaching of the Zumkehr reference, if the write command 522B was sent at time T1A, the write data associated with that command would not have been sent at time T2B to T3B as indicated by the Examiner. And if the write data was sent any time after time T2B to T3B, there would be a data collision either on the RAMBUS data bus or the SDRAM data bus.

For all of the reasons stated above, the rejection of claims 40-43 should be reversed.

Respectfully submitted,

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